IN THE CLAIMS

Please cancel claims 5-12 without prejudice or disclaimer and amend claims 1-4 as set forth below.

1. (Currently Amended) A non-volatile semiconductor memory device [of] having a memory cell array of aligning plural numbers of memory cells [semiconductor memory element] in a matrix-like manner, each of said [element] memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed [of semiconductor connecting] between said source region and said drain region, and in said semiconductor substrate;

a gate electrode [made of either one of metal and semiconductor,] for controlling potential of said channel region; and

plural numbers of charge storage [regions] grains formed [in vicinity of said channel] between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator, wherein:

a first [semiconductor] memory cell and a second [semiconductor] memory cell neighboring with each other in the direction of channel length share said source region in common.

2. (Currently Amended) A non-volatile semiconductor memory device [of] having a memory cell array of aligning plural numbers of memory cells [semiconductor memory element] in a matrix-like manner, each of said [element] memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed [of semiconductor connecting] between said source region and said drain region, and in said semiconductor substrate;

a gate electrode [made of either one of metal and semiconductor,] for controlling potential of said channel region; and

plural numbers of charge storage [regions] grains formed [in vicinity of said channel] between said gate electrode and said channel region, and isolated from said gate

electrode and said channel region and with each other by an insulator, wherein:

a first [semiconductor] memory cell and a second [semiconductor] memory cell neighboring with each other in the direction of channel length share said source region in common; and

said second [semiconductor] cell shares said drain region in common with a third [semiconductor] memory cell neighboring in the direction of channel length therewith.

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3. (Currently Amended) A non-volatile semiconductor memory device [of] having a memory cell array of aligning plural numbers of memory cells [semiconductor memory element] in a matrix-like manner, each of said [element] memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed [of semiconductor connecting] between said source region and said drain region, and in said semiconductor substrate;

a gate electrode [made of either one of metal and semiconductor,] for controlling potential of said channel region; and

plural numbers of charge storage [regions] grains formed [in vicinity of said channel] between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator, wherein:

plural numbers of [a layout of] cell separation regions in [of] said memory cell array [is in a rectangular shape,] are aligning [them] in parallel to each other, substantially;

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plural numbers of [a layout of] word lines for connecting said gate electrodes of said [semiconductor] memory cells [is in a rectangular shape,] are aligning [them] in parallel to each other, substantially;

said [semiconductor] memory cell [has such structure that it] shares a diffusion layer [region] of said source region in common with only one memory [(1)] cell neighboring in the direction of channel length therewith;

each source region [said source lines] of at least three [(3)] of said [semiconductor] memory cells neighboring in the direction of channel width are connected with one

another through a [either one of diffusion layer wiring and] metal wiring; and

said [rectangular] cell separation [regions] region is perpendicular [of aligning in parallel to each other and said rectangular diffusion layers of aligning in parallel to each other are in parallel] to said metal wiring [each other], substantially, and said [rectangular] cell separation region is [of aligning in parallel to each other and said word lines aligning in parallel to each other are] perpendicular to said word line, substantially [each other in a positional relationship therebetween].

4. (Currently Amended) A non-volatile semiconductor memory device [of] having a memory cell array of aligning plural numbers of memory cells [semiconductor memory element] in a matrix-like manner, each of said [element] memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed [of semiconductor connecting] between said source region and said drain region, and in said semiconductor substrate;

a gate electrode [made of either one of metal and semiconductor,] for controlling potential of said channel region; and

plural numbers of charge storage [regions] grains formed [in vicinity of said channel] between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator, wherein:

plural numbers of [a layout of] cell separation regions [of] in said memory cell array are [is] in a rectangular shape, aligning [them] in parallel to each other, substantially;

plural numbers of [a layout of] word lines for connecting said gate electrodes of said [semiconductor] memory cells are [is in a rectangular shape,] aligning [them] in parallel to each other, substantially;

[said semiconductor memory cell has such structure that] plural numbers of said source regions thereof are connected with each other through [the] a diffusion layer wiring [layers];

plural numbers of diffusion layer wirings [a layout of the diffusion layers connecting the plural numbers of said

source regions is in a rectangular shape,] aligning [them] in parallel to each other, substantially; and

said [rectangular] cell separation [regions] region is perpendicular [of aligning in parallel to each other and said rectangular diffusion layers of aligning in parallel to each other are in parallel] to said diffusion layer wiring [each other], substantially, and said [rectangular] cell separation region is [of aligning in parallel to each other and said word lines aligning in parallel to each other are] perpendicular to said word line, substantially [each other in a positional relationship therebetween].

5. - 12. (Canceled)